In The Claims:

This list of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method for manufacturing metal lines of a semiconductor device, the method comprising the steps of:

forming a first interlayer insulating film exposing a top portion of a lower metal line on a semiconductor substrate;

forming a stacked structure of a first etch barrier film, a second interlayer insulating film, a second etch barrier film, a third interlayer insulating film and an anti-reflection film;

etching the stacked structure to form a via contact hole exposing a portion of the first etch barrier film on the lower metal line;

removing the exposed portion of the first etch barrier film to expose the lower metal line;

forming a photoresist film on the entire surface of the exposed lower metal line, the via contact hole, and the remaining antireflection film;

subjecting the photoresist film to an exposure and development process using an upper metal line mask to form a photoresist film pattern for defining an upper metal line region, wherein the photoresist film pattern further fills a portion of the via contact hole to cover the exposed lower metal line;

etching the anti-reflection film and the third interlayer insulating film using the photoresist film pattern as a mask to form the upper metal line region;

removing the photoresist film pattern; and

after the photoresist film pattern is removed, forming an upper metal line contacting the lower metal line by filling the upper metal line region.

2. (Original) The method according to claim 1, wherein the first and the second etch barrier films comprise a film selected from the group consisting of SiN film, SiC film and SiCN film, respectively.

3. (Previously Presented) The method according to claim 1, wherein the second and the third interlayer insulating films comprise a film selected from the group consisting of a silica-base low-k film and a silica-base porous low-k film, respectively.

4. (Previously Presented) The method according to claim 1, wherein the second and the third interlayer insulating films comprise a film selected from the group consisting of an oxide film, an organic low-k film, an organic porous low-k film and combinations thereof, respectively.

5. (Original) The method according to claim 1, wherein the anti-reflection film comprises a SiON inorganic anti-reflection film.

6. (Original) The method according to claim 1, wherein the step of etching the anti-reflection film and the third interlayer insulating film is a plasma etching process using a mixture gas of $CF_4/O_2/Ar$.

7. (Original) The method according to claim 6, wherein the step of removing the photoresist film pattern in the via contact hole is performed in in-situ manner.